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Silicon as a Millimeter-Wave Monolithically Integrated Substrate - A New Look

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Silicon as a Millimeter-Wave Monolithically Integrated Substrate—A New Look*

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Abstract—Materials suitable for use as monolithic substrates are summarized. A study of the properties of *silicon* substrates as transmission line media shows that serious consideration should be given to them for use *at mm*-wave frequencies. It is concluded that for silicon resistivities of 2000 ohm-cm or greater, microstrip loss in *silicon* at mm-wave frequencies is only slightly higher than that in GaAs or alumina. The cross section width of *a transmission* line represents an appreciable part of a wavelength when microstrip is used as an impedance *transformer* at mm-wave frequencies. Therefore, substrate thickness (using the latest dispersion characteristics) is *especially* considered in circuit design. These effects on the design of 3-dB interdigitated and branch-line *couplers* are demonstrated.

Fabrication of silicon IMPATT diodes operating up to 200 GHz has been accomplished by novel techniques that maintain the silicon's high resistivity. We report on diodes yielding 25 mW cw at 102 GHz, 16 mW cw at 132 GHz, and 1 mW at 195 GHz. The techniques described are ion implantation, *laser annealing*, unique secondary-ion mass spectrometry (SIMS) profile diagnostics, and novel wafer thinning. *The utilization* of these technologies paves the way for the processing of silicon monolithic mm-wave integrated *circuits*.

1. Introduction

One of the major goals of microwave research in the past several years

* This paper is based *in* part on excerpts from our papers in the IEEE Trans. MTT[3] 1982 and in the SPIE Proceedings of the Conference on Integrated Optics and Millimeter and Microwave Integrated Circuits Vol. 317, 1982.[4]

has been the development of the technologies needed to fabricate monolithic microwave (mm-wave) integrated circuits. This goal has now been attained. Since the introduction of the microstrip for use in microwave integrated circuits[1] in 1965, the pros and cons of hybrid versus monolithic circuits have been debated. Although still an item of contention, the role of hybrid technology below 36 GHz seems to be assured in present planning. However, the potential advantages of monolithic circuits above 40 GHz make their use at even higher frequencies the most favored approach for future applications.[2] Parasitic inductance, normally encountered in forming devices and circuits, is reduced and controlled in the monolithic approach, making it a most attractive technique for use in millimeter-wave circuits. The silicon IMPATT diodes are the only solid-state microwave devices presently capable of delivering the required power output of hundreds of mill-watts at 100 GHz. High-resistivity bulk silicon is an adequate substrate for use in EHF monolithic integrated circuits, provided modern silicon processing technologies such as ion implantation, laser annealing, and wafer thinning are utilized to fabricate the ICs. For example, the processing temperature must not exceed 800°C if the required high resistivity of the bulk silicon starting material is to be preserved. We will consider:

(1) the pros and cons of materials considered for use as monolithic substrates at mm-wave frequencies;
(2) the properties of microstrip, with attention to both dielectric and conductor losses;
(3) the effect of shorter wavelengths (with increasing frequency) as the wavelengths become comparable with microstrip cross section;
(4) a novel technology for the fabrication of mm-wave devices utilizing ion-implantation, laser annealing, and unique SIMS diagnostics.

2. Materials for Monolithic Approaches

Our discussion of the possible materials for monolithic approach in EHF is based on the premise that the circuit will be processed around available devices. The silicon IMPATT currently dominates as a power device at EHF; therefore, silicon monolithic transmitters should be seriously considered.

The following are the advantages and the disadvantages of various substrate materials, for the monolithic approach.

Silicon-on-Sapphire

Sapphire is one of the best insulators for use as a transmission substrate, and the suggestion to grow silicon on it for monolithic microwave circuits dates back to 1966.[6,7]

(a) Advantages
Silicon is used only where devices are included, while the sapphire, a superior insulating substrate, is present as the passive substrate.

(b) Disadvantages
Difficult to contact ground plane; via holes are required.
Silicon grown on sapphire to date has not proven suitable for high-frequency devices.

This technique is not sufficiently advanced for consideration at this time.

Gallium Arsenide

Gallium Arsenide is the material presently under consideration for lower-frequency monolithically integrated circuits. Its use at frequencies below 35 GHz is under development.[8]

(a) Advantages
Above 40 GHz: Schottky-barrier mixers, IMPATTs, and Gunn devices have been made.
Below 45 GHz, FETs up to K-band have been developed.
Good insulator material (up to 10^8 Ω-cm).

(b) Disadvantages
Its use has not yet become an established technology, compared to that of silicon.
Above 40 GHz, power devices are not thus far within the state-of-the-art.
Large wafers are not yet readily available.
Heat conduction is one-half that of silicon.

Gallium arsenide substrates are not yet suitable for use in high-power mm-wave transmitter modules, but they may be ideal for i-f and receiver modules. It is worthwhile mentioning that silicon could also be used for the receiver module, excluding the local oscillator which, at this point, has to be a Gunn device.

Silicon

The use of high-resistivity silicon as a substrate for microwave circuits was first seriously investigated in 1965. Circuit losses introduced by the dielectric were found to be minimized by a high-resistivity substrate. Measurements on 1400-Ω-cm silicon at 10 GHz have yielded respectable losses for microstrip circuits.[5] Silicon substrates of 2000 to 10,000 Ω-cm are presently available, the use of which further minimizes substrate loss. However, because the high temperatures required in device processing destroys its intrinsic properties, the use of silicon as a substrate was

abandoned. Today, it *is possible* to use ion implantation and selective laser annealing to create devices without increasing substrate temperature, and the high-resistivity silicon can, therefore, be used as a substrate material for millimeter-wave circuits. Since silicon of high resistivity can be obtained and maintained, a new range of possibilities is open to use, particularly for mm-waves. The advantages and disadvantages of using silicon as a basic material for monolithic circuits are listed below.

(a) Advantages
Silicon use is based on a well-established technology.
Above 35 GHz, high-power IMPATTs, PIN diodes, varactors, and devices for transmitting circuits are within the state-of-the-art.

(b) Disadvantages
Intrinsic insulating qualities are degraded by temperatures above 800°C.
Bipolar devices are not achievable above X-band.
Gunn devices are not feasible.

We conclude that through the use of modern processing technology, silicon once again offers exciting possibilities, particularly for monolithic millimeter-wave transmitters and amplifiers.

The use of silicon is particularly attractive because we have successfully fabricated high-frequency silicon IMPATT devices using selective ion implantation and laser annealing, and we have obtained state-of-the-art devices without necessarily raising the temperature of the whole substrate. Intrinsic silicon can now be used, and the high resistivity can be maintained throughout the device fabrication steps. Thus, the main objections to the use of silicon have been removed. We have examined the properties of silicon and the transmission lines obtained using intrinsic Si as a substrate for microstrip from 40 to 100 GHz. In a way, a new world for monolithic mm-wave circuits has been reopened.

3. Microstrip Lines on Intrinsic Silicon

A technique explored in the early days of MIC technology was that of microstrip lines on silicon. In 1965, T. M. Hyltin[5] demonstrated reasonable losses at 10 GHz using silicon of 1400-Ωcm resistivity.

Microstrip on silicon has been examined in many laboratories. At RCA in 1973, Sobol and Caulton[2] presented an analysis of silicon microstrip properties including conductor and substrate losses. Gopinath[9] analyzed microstrip, including radiation losses when GaAs substrates were used. Typical results are displayed to demonstrate silicon microstrip properties. Fig. 1 (Fig. 9 of Ref. [2], modified) demonstrates the relative

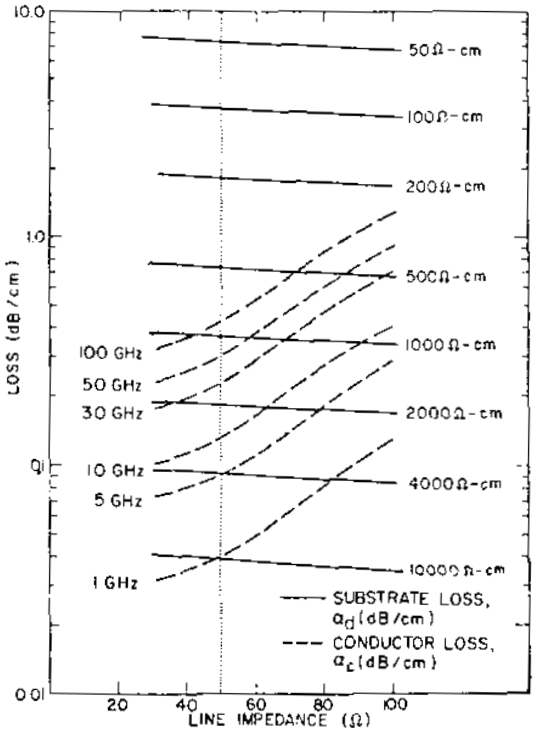


Fig. 1—Conductor and substrate losses (in dB/cm) of microstrip lines on Si substrates.

contributions of substrate and conductor losses versus characteristic impedance. We conclude that (1) at the higher frequencies (>30 GHz), the conductive loss dominates, (2) the substrate loss is independent of frequency, and (3) if the resistivity of the substrate is 2000 Ωcm or greater, it will not contribute significantly to the total loss. Fig. 2 (Fig. 11 of Ref. [2]) shows the sum of the conductive and Si substrate losses versus frequency for 50-Ω lines on 10-mil-thick Si and GaAs substrates. A comparison between theoretical and measured losses[5] on a silicon substrate microstrip is shown in Fig. 3. The agreement is excellent. Fig. 4 (Fig. 2 of Ref. [4]) demonstrates the measured total loss (up to 18 GHz) of a 50-ohm line on an 8-mil-thick (5000 ohm-cm) silicon substrate, indicating a variation of 65% from the calculated values shown in Fig. 2.

We use the equations presented by Schneider[10] to compare the loss factor α of our Figs. 1 and 2 with the Q of a resonator:

$$Q = \frac{20\pi}{\ln 10} \frac{1}{\alpha\lambda}$$

where λ is the guide wavelength. Pertinent data are

Fig. 1 (10-mil Si): 50 GHz, α_c = 0.3 dB/cm, λ = 0.23 cm[11], $\alpha\lambda$ = 0.069 dB, Q = 395;

Fig. 2 (10-mil Si): 50 GHz, α = 0.33 dB/cm, λ = 0.23 cm, $\alpha\lambda$ = 0.076 dB, Q = 359;

Fig. 5 (4-mil Si): 60 GHz, α = 1.78 dB/cm, λ = 0.19 cm, $\alpha\lambda$ = 0.34 dB, Q = 80.

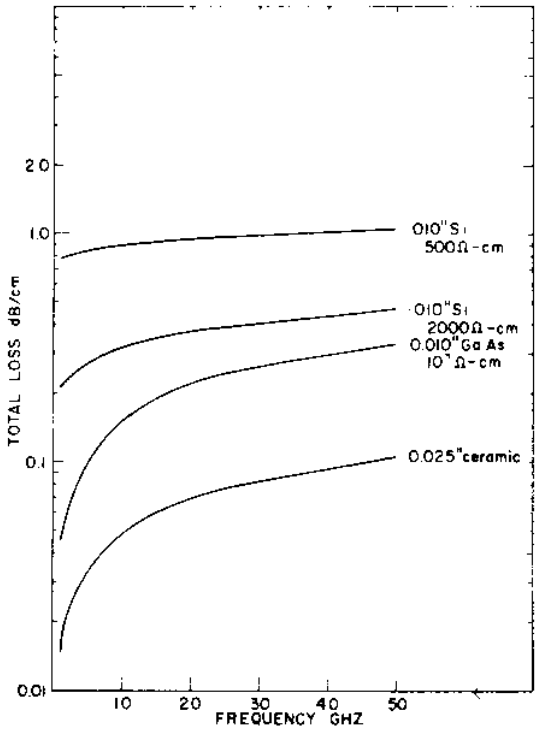


Fig. 2—Loss (in dB/cm) as a function of frequency for 50-ohm microstrip lines on Si, GaAs, and ceramic substrates. Loss includes both α_c and α_d.

The dielectric Q_d is related to the resistivity ρ by[12]

$$Q_d \sim \omega\rho\epsilon \approx \omega/\omega_d,$$

where ϵ is the dielectric permittivity for silicon ($\epsilon = 11.8 \times 8.85 \times 10^{-14}$ farads/cm). ω_d may be defined as a dielectric relaxation frequency,

$$\omega_d = \frac{1}{\rho\epsilon}.$$

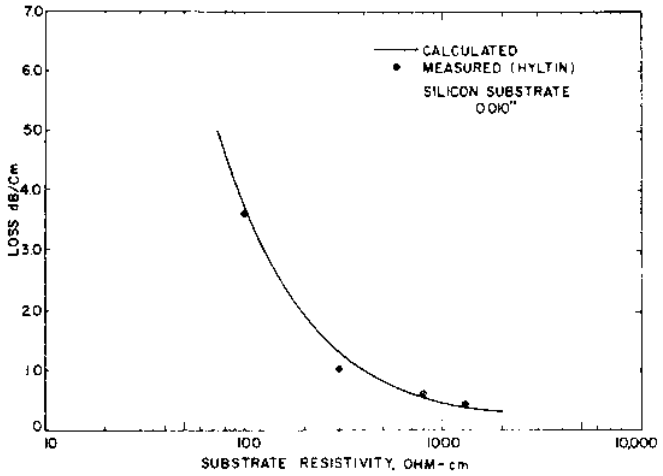


Fig. 3—Loss (in dB/cm) as a function of substrate resistitivity for 50-ohm microstrip line on Si substrate (measurements and calculations for 10 GHz). From Ref. [5].

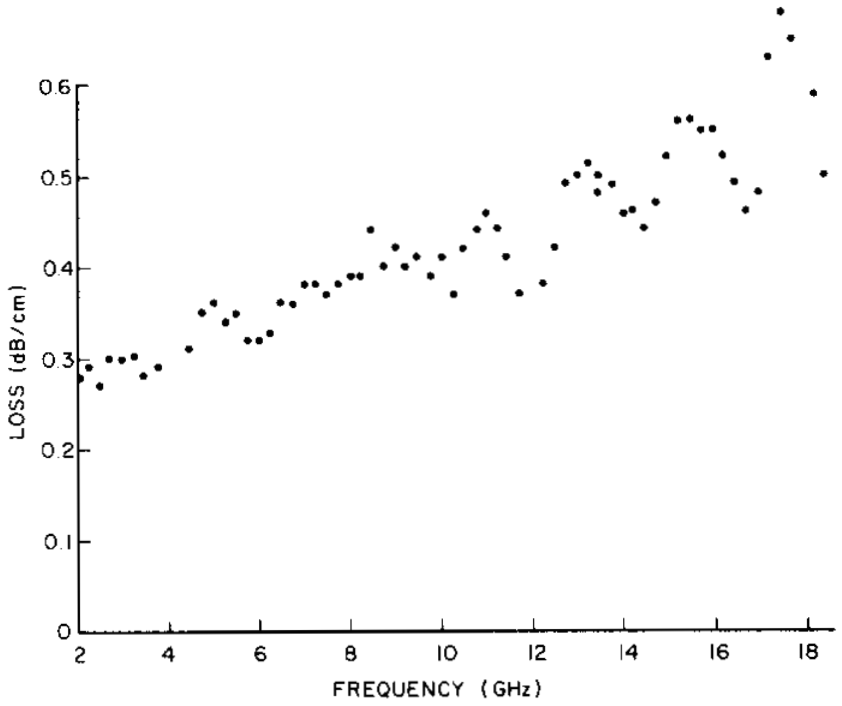


Fig. 4—Measured loss versus frequency of 50-ohm microstrip line. Substrate 5000 ohm-cm silicon, 8-mil thick, Au line 6.4-mil wide.

Above the frequency ω_d, the substrate appears primarily as a resistive material. Fig. 6 shows $f_d = \omega_d/2\pi$ for GaAs and Si, as a function of temperature. The figure displays an estimate of a lower limit on the operating frequency. We are using Fig. 6 to compare the measured change in loss as a function of temperature via the previous equations

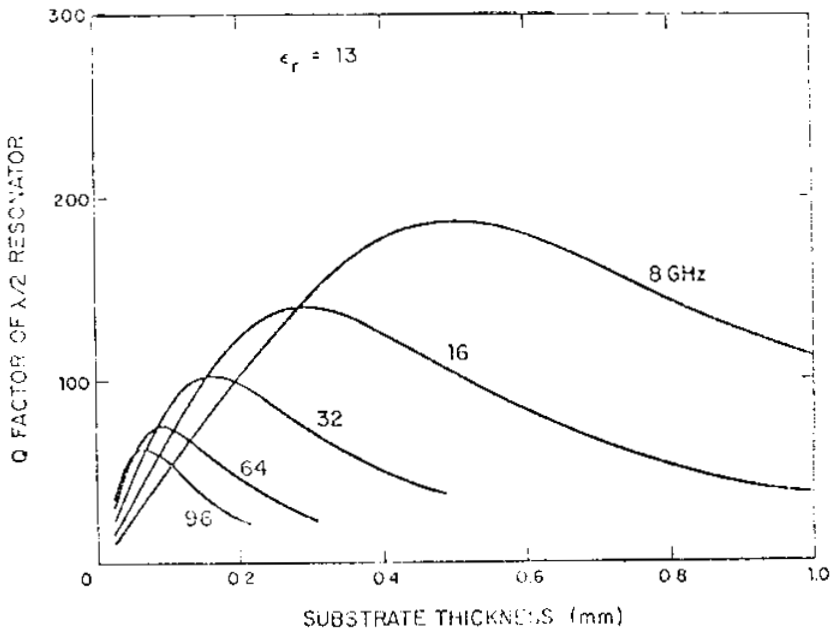


Fig. 5—*Q* factor versus substrate thickness for 50-Ω transmission lines. Reprinted from Gopinath[9] (Fig. 3e of Ref. [9], IEEE 1981).

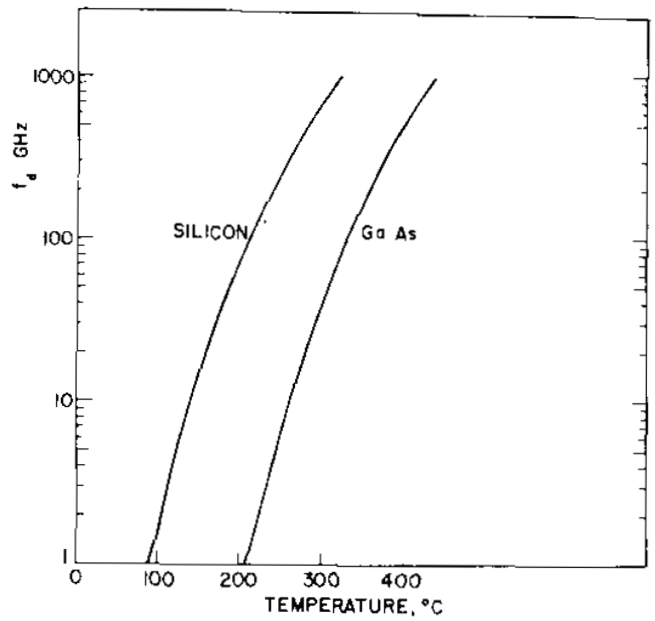


Fig. 6—Dielectric relaxation frequency of Si and GaAs substrates as a function of temperature.

of Q_d and ω_d. For example, at 60 GHz, for ρ = 10,000 Ω-cm, Q_d = 3937 and for ρ = 2,000 Ω-cm, Q_d = 787.

The relationship between Q and the dielectric loss tanδ takes into account the effective dielectric constant $\epsilon_{r_{eff}}$[13]:

$$\frac{1}{Q_d} = \frac{\dfrac{1}{\epsilon_{r_{eff}}} - 1}{\dfrac{1}{\epsilon_r} - 1} \tan \delta.$$

This relationship occurs because ϵ_r does not completely fill the media. $\epsilon_{r_{eff}}$ = 6.755 and for Q_d = 3937,

$$\tan\delta = 2.7 \times 10^{-4}$$

while for Q_d = 787,

$$\tan\delta = 1.35 \times 10^{-3}.$$

The attenuation is related to the substrate parameters by

$$\alpha_d = \frac{20\pi}{\ln 10} \frac{1}{Q_d \lambda}$$

$$\alpha_d = \frac{10}{\ln 10} \frac{\sqrt{\epsilon_{r_{eff}}}}{\rho e\ (3 \times 10^{10})} \text{ dB/cm}.$$

α_d is thus almost independent of frequency, although tanδ and Q_d are not. For example, for ρ = 2000 Ω-cm, α_d = 0.18 dB/cm, as shown in Fig. 1. Note that in Fig. 2, the total loss of 50 GHz only increases from 0.33

dB/cm to 0.47 dB/cm with a decrease of dielectric resistivity from 10^7 to 2×10^3 Ω-cm.

Fig. 5 is a plot of Q for various frequencies (including radiation) versus substrate thickness for GaAs, the loss of which is close to that of silicon at high frequencies (taken from Ref. [7], Fig. 3e). For operation at 60 GHz, a thickness of 0.1 mm, or 4 mils, will allow the achievement of a Q of 80, corresponding to an α of 0.62 dB/cm, as shown previously. This necessitates the use of a 3-mil-wide metal for a 50-Ω line, a disadvantage for reproducibility and accuracy. When the circuit is shielded in a waveguide below cutoff, radiation poses no problem and 10-mil or thicker substrates can be used. Fig. 2 would then apply.

The figures presented here allow us to draw some conclusions. At low frequencies, silicon microstrip for microwave integrated circuits incurs great losses compared to alumina and GaAs. Fig. 1 shows that for frequencies below 30 GHz, the substrate loss of silicon (2000 Ω-cm) is equal to or greater than the conductor losses; for GaAs, which has a resistivity of greater than 10,000 Ω-cm, the conductor loss at 1 GHz is far greater than the substrate loss. Fig. 2 shows that the total losses of silicon and GaAs microstrip are comparable above 40 GHz. Two thousand ohm-cm (or greater) silicon is a viable substrate for frequencies above 30 GHz, where conductor and radiation losses dominate. The above conclusion assumes that the high-resistivity property can be maintained throughout all the processing steps. At RCA Laboratories, we have successfully processed and fabricated diodes using very thin wafers, as will be described. This process involves ion-implantation and laser-annealing, techniques that do not alter substrate resistivity.

A silicon dielectric, or image line,[14] has very low loss at high frequencies. Therefore, it is suitable for frequencies above 100 GHz. Techniques to integrate this image line with microstrip devices can lead to feasible monolithic components.

Our experience has shown that at frequencies greater than 30 GHz, the use of silicon microstrip is acceptable provided resistivities of 2000 Ω-cm and higher can be maintained. Modern technology makes it possible to fabricate devices without deterioration of the material resistivity, which was impossible in 1965 when silicon monolithic circuits were first proposed for microwaves. The use of silicon microstrip is now feasible, therefore, from 30 GHz and above with reasonable loss, and dielectric and image lines are available to extend the frequency range beyond 100 GHz. Measurements of microstrip losses at 60 GHz are of critical importance. It is well known that the microstrip is a relatively high-loss transmission line when compared with waveguides, especially on a per-unit-length basis. At high frequencies, however, the loss per wavelength is small due to the physical length.

Transmission lines at high frequencies exhibit a new problem. As the frequency increases, the wavelength shortens. The cross-sectional width W (nearly constant or increasing because of dispersion) thus becomes an important fraction of a wavelength, with resultant phase changes across the transverse dimension. Some of the first circuits built under this constraint are 3-dB couplers that we are studying for use as a key element for a two-stage amplifier in silicon.

An initial coupler being considered is the Lange coupler (interdigital). This is the widest bandwidth microstrip approach amenable for batch fabrication. The circuit design and configuration of a Lange coupler are shown in Fig. 7. The design of the interdigitated coupler has been successfully demonstrated at Ka-band and can be scaled to a chosen frequency. The length of the hybrid is $\lambda/4$. The width of the line and spacing between the lines, W and S, respectively, are determined for given substrate thicknesses using the Bryant and Weiss tables and standard techniques. At the RCA Microwave Technology Center, we have developed a computer optimization routine that is very useful in predicting the performance of the hybrid. For a four-line interdigitated hybrid on a 200-μm-thick Si substrate ($\epsilon_r = 11.8$), the following results are obtained:

$W/H = 0.065$; $W = 13\ \mu$m and $H = 200\ \mu$m;

$S/H = 0.07$; $S = 14\ \mu$m and $H = 200\ \mu$m; for $\lambda/4$ at 45 GHz.

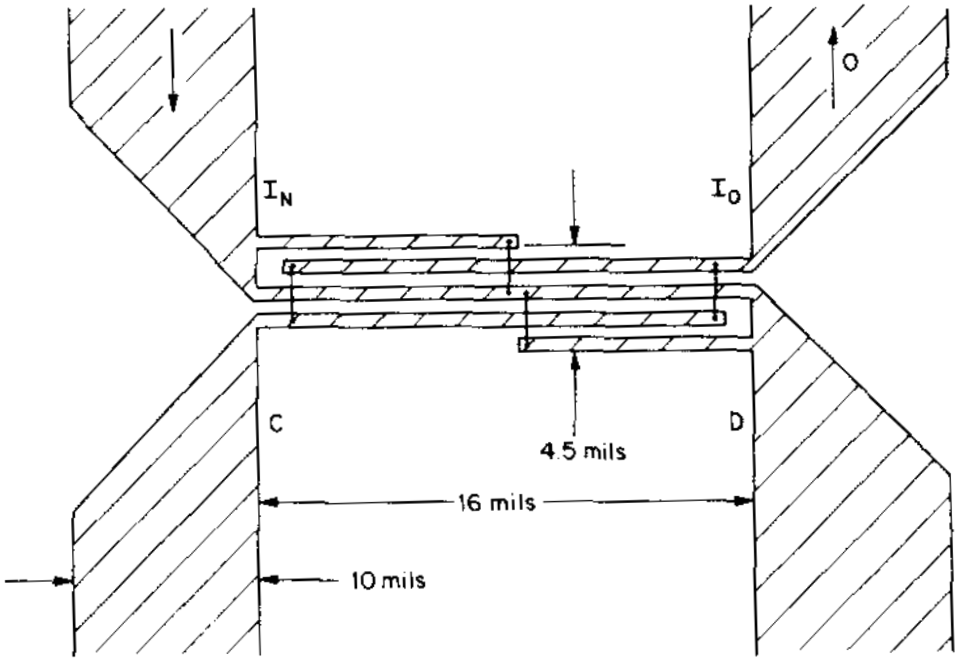


Fig. 7—A Lange coupler for 60-GHz applications.

Fig. 7 represents the coupler design for use on silicon substrate at 60 GHz. The important problems illustrated (the coupler is drawn to scale) are as follows. (1) Although the bonded points are to be at the same potential, the cross section is large compared to a quarter wavelength. The coupler's performance is uncertain at this time, because of the standing-wave pattern in the cross-sectional area. (2) The size of the lines (0.5 mils width and separation) makes the coupler difficult to fabricate.

Another coupler being considered is the quadrature branch-line coupler. It consists of two 50-ohm and two 35.3-ohm lines, each $\lambda/4$ long. For this coupler to operate at high frequencies, the $\lambda/4$ cross-sectional width should be large, and rectangular breaks are to be avoided. Fig. 8 illustrates the respective dimensions of a microstrip line and Fig. 9 shows a possibly-acceptable design on 6-mil silicon, drawn to scale. Results of this coupler on 8-mil alumina at 50 GHz have been reported.[15]

Yamashita, et al,[16] have proposed the latest high-frequency microstrip dispersion curves based on theory as well as experiment. These curves have been incorporated into a computer program, whereby we calculate impedance and width as a function of ϵ_r (dielectric constant) and of substrate height H. Table 1 lists characteristics for $\lambda/4$, cross-section W, and a figure of merit L/W, for various substrates and thicknesses with the objective of verifying if 3-dB couplers can be fabricated. The higher the figure of merit, the longer the microstrip line, L, compared to the cross sectional width, W (Fig. 8). Fig. 10 is the scale drawing of a 60-GHz coupler on 10-mil silicon. The figure of merit, 1.6, is not promising and as seen, the lines merge into one another. However, the coupler on 6-mil Si (Fig. 9) has a figure merit of 3.1.

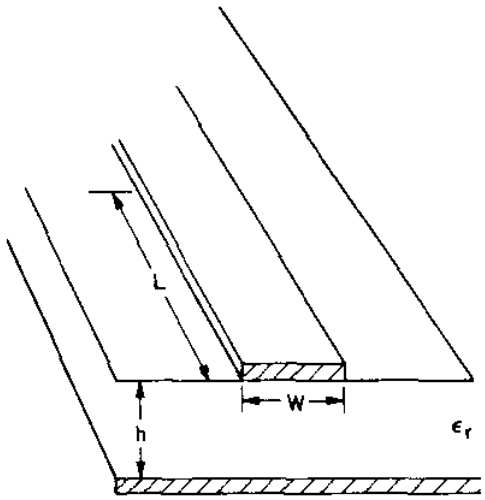


Fig. 8—Dimensions of a microstrip line.

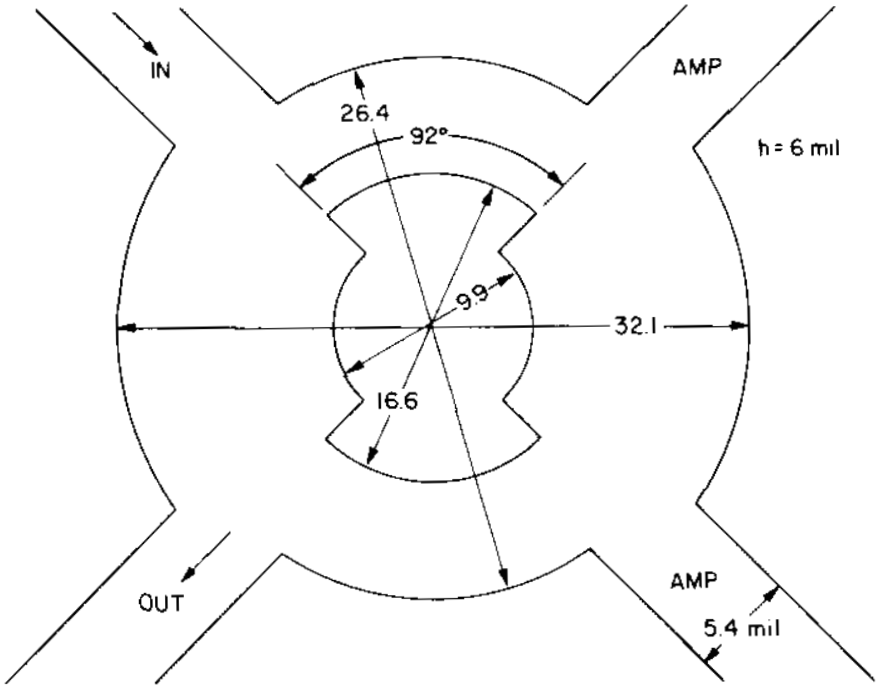


Fig. 9—Design of a branch-line coupler on 6-mil-thick silicon substrate (dimensions in mils).

Table 1—Line Width for 50-Ohm and Quarter Wavelength Lines for Different Substrates (Dimensions in Mils)

Substrate	Freq.	Height	Width	L = λ/4	L/W
Silicon (ϵ_r = 11.8)	60 GHz	6	5.4	16.8	3.1
		8	7.6	16.4	2.2
		10	9.8	16.1	1.6
Quartz (ϵ_r = 3.8)		10	25.8	27.3	1.1
Quartz	44 GHz	10	25	38	1.5
		6	14	38	2.8
Alumina (ϵ_r = 10)		10	11	24	2.2
		8	8.5	25	2.8
		5	5	26	5.1

5. Vapor-Phase Grown Silicon Epitaxial Multi-Layer IMPATT Diode Structures

We have successfully fabricated the following structure as shown in Fig. 11:

Substrate: 3×10^{19} (arsenic-doped)
First epi film: 0.3 μm of 3×10^{17} (n) (arsenic-doped)
Second epi film: 0.3 μm of 2×10^{17} (p) (boron-doped)

An ion implantation (not shown) completes the double-drift IMPATT structure.

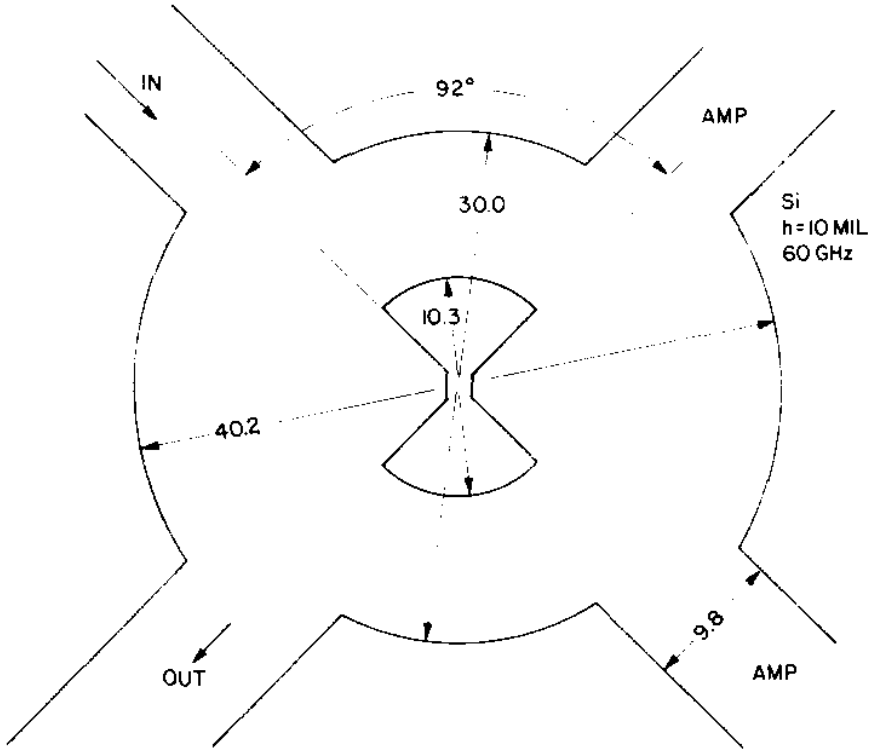


Fig. 10—Design of a 60-GHz branch-line coupler on 10-mil-thick silicon substrate (dimensions in mils).

A. Deposition

Vapor-phase, epitaxial-silicon, single and multi-layer IMPATT diode structures,[17-21] as shown in Figs. 11 and 12, are deposited on a ⟨111⟩ oriented substrate, in a hydrogen atmosphere, using the conventional

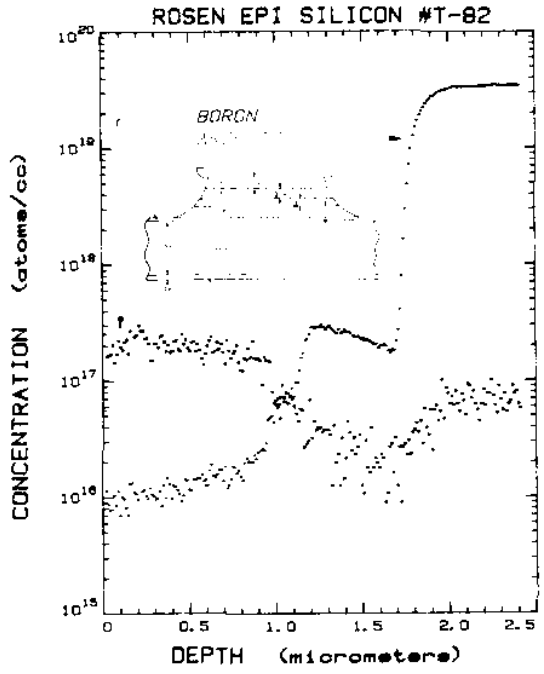


Fig. 11—SIMS depth profiles of epi-grown n and p on n^+ arsenic-doped substrate.

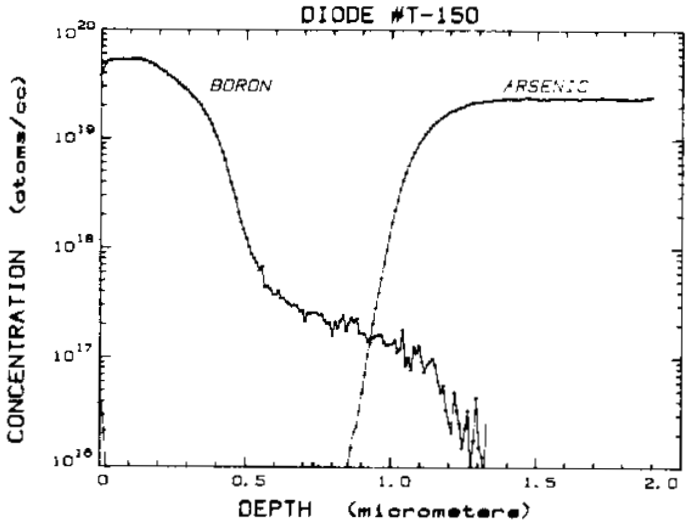


Fig. 12—SIMS depth profiles of epi-grown p and ion-implanted p^+ on n^+ arsenic-doped substrate.

silane (SiH_4) decomposition method. All the silicon layers are deposited at a substrate temperature ranging from 1000°C to 1050°C. Diborane or arsine gas is introduced during the epitaxial growth process to achieve the desired impurity concentration in the respective layers.

B. Growth

The substrates' back surface and side edges were coated with 2000 Å of deposited oxide. The substrates were heated to approximately 1150° and etched with HCl (1% HCl for 5 minutes). The temperature was then dropped to approximately 1050°C and the first epi-layer was grown. The system was then purged for all reaction gases (at 1050°C) before the second epi-film was grown. The adjustment of crystal growth parameters, using impurity concentration profiles by SIMS, have led to sharp transitions (Fig. 13). The concentration varies from 3×10^{19} atoms per cc in the substrate to 2×10^{17} atoms per cc in the epitaxial layer over a distance of only 3000 Å.

6. Device Fabrication by Ion Implantation and Laser Annealing

6.1 Single Drift Structure

As discussed above, the conventional fabrication technique is via epitaxy. The n layer, followed by p and p^+ layers, are grown in succession upon an n^+ substrate which serves as a handle during the fabrication (this substrate is partially etched away just before the final Cr-Au metallization). When the design frequency of the IMPATT exceeds 140 GHz, the doping profile requirements (e.g., junction abruptness and uniform layer thickness) are difficult to meet using this epitaxial technique.

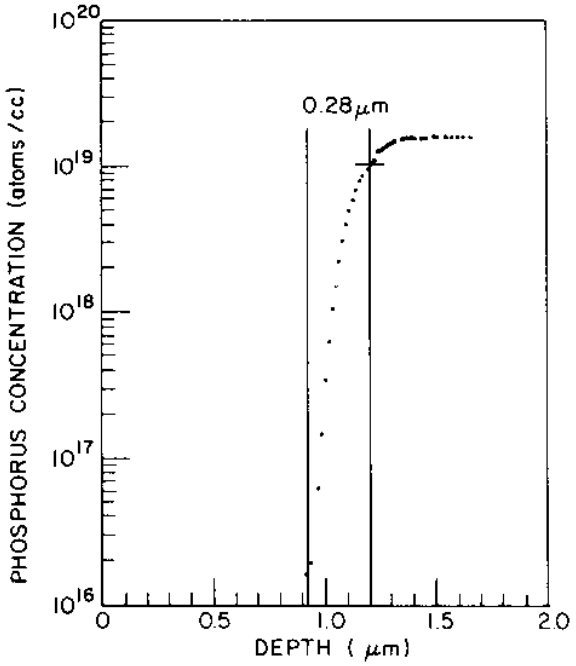


Fig. 13—Impurity concentration profile in transition region.

A novel application has been proposed[22] that uses both ion-implantation and laser annealing techniques to achieve uniformity and reproducibility of the closely-spaced junctions. The single-drift IMPATT was successfully processed as a vehicle for the more difficult double-drift structure. First, an n-layer with doping concentration of about 5×10^{16} cm^{-3} is grown at 1050°C on a (111) oriented n^+ silicon substrate using conventional silane pyrolysis. The thickness of this n-epi layer is 2 μm. Next, two ion implants are carried out under the following conditions:

(1) n region: ^{31}P implant at 500 keV with a fluence of 1×10^{13} cm^{-2}
(2) p^+ region: ^{11}B implant at 50 keV with a fluence of 2×10^{15} cm^{-2}

Typical SIMS analyses of these implants before and after annealing are shown in Figs. 14(a) and (b), respectively. After the above ion-implants, the wafer can be either thermally annealed at 1000°C for 15 minutes in dry N_2 (after depositing 0.5 μm SiO_2 as capping) or laser annealed.

The wafer is then metallized on the p^+ side with Cr-Au and electroplated with 25-μm-thick copper to form the heat sink. Another layer of gold, 2-μm thick, can be plated upon the copper heat sink. This metallization also serves as a handle for subsequent processing. At this point, the n^+ silicon substrate can be completely or partially removed by the procedure for wafer thinning, described in the next section.

Next, the n^+ layer is formed by a 950 keV $^{31}P^+$ ion implant with a fluence of 3×10^{15} cm^{-2}. This implanted layer 0.95 μm in depth is then laser annealed. The laser annealing heats the material to a depth of only

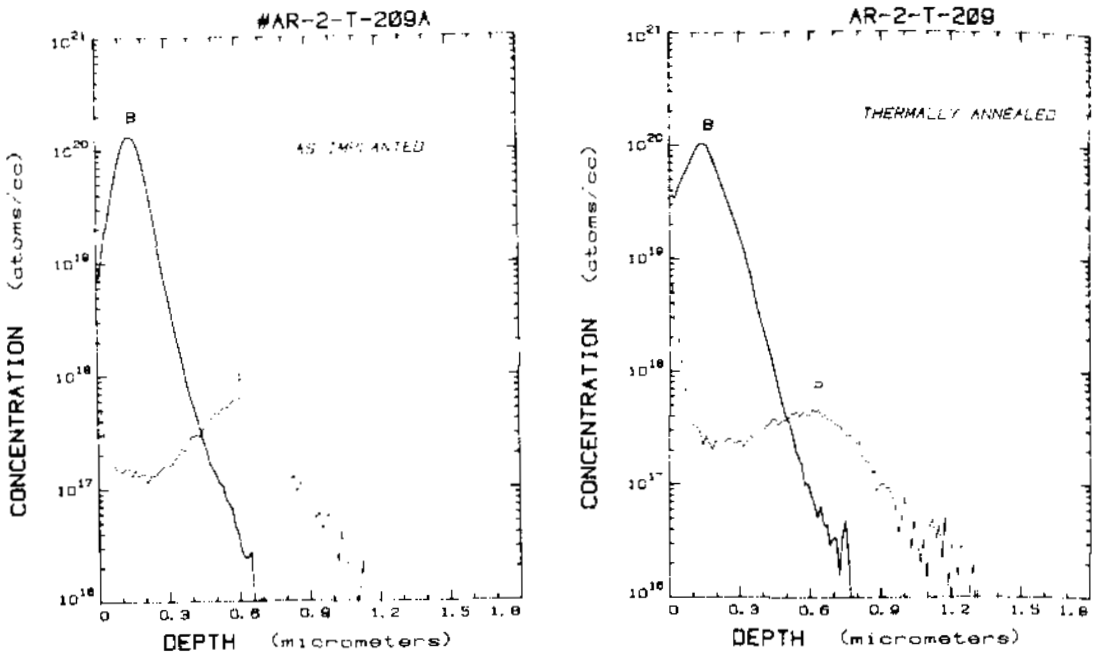


Fig. 14—Results (measured by SIMS) obtained on implanting ^{31}P and ^{11}B in silicon before and after annealing.

one micron and for a very short time (~1 μsec). Thus, there is no deleterious effect at the metal-silicon interface (2 μm away), and profile redistribution is minimized. Laser annealing is necessary here because, at this point in the processing sequence, the above device structure (with one side metallized) cannot be thermally annealed.

The n^+ contact layer is first evaporated with Cr-Au. Then, an array of gold dots is electroplated through a photoresist mask. The unplated metallization is removed, and mesa diodes are formed by etching completely through the unplated area of the semiconductor layer. Finally, the diodes are separated, and each diode, with its attached copper heat sink, is tested. I-V characteristics are shown in Fig. 15. Figs. 16(a), (b), and (c) demonstrate the possibility of processing devices, when even higher penetration is needed, by using higher energy levels.

6.2 Double-Drift Structures

For application of the double-drift diode at around 140 GHz, a mm-wave IMPATT diode with symmetrical structure and total active layer thickness of 0.5 μm is desired. Such a device requires four implants instead of only three. The proposed device is to have a total thickness of 1.5 μm. Hence, an n-epi layer of 1.5 μm thickness and doping concentration of 1×10^{16} cm^{-3} is first grown on an (111)-oriented n^+ silicon substrate. The doping concentration of the n-epi layer is not critical in this case and can be varied within a factor of 2 or 3 without seriously affecting the performance of the finished device. However, the thickness

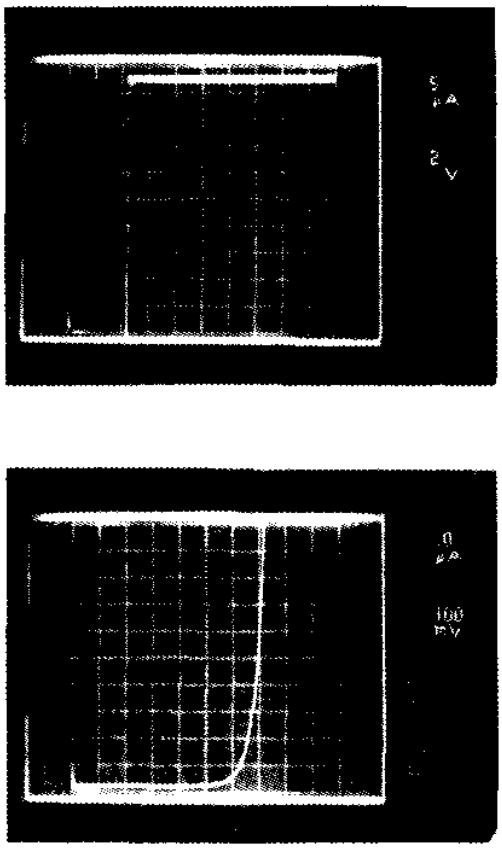


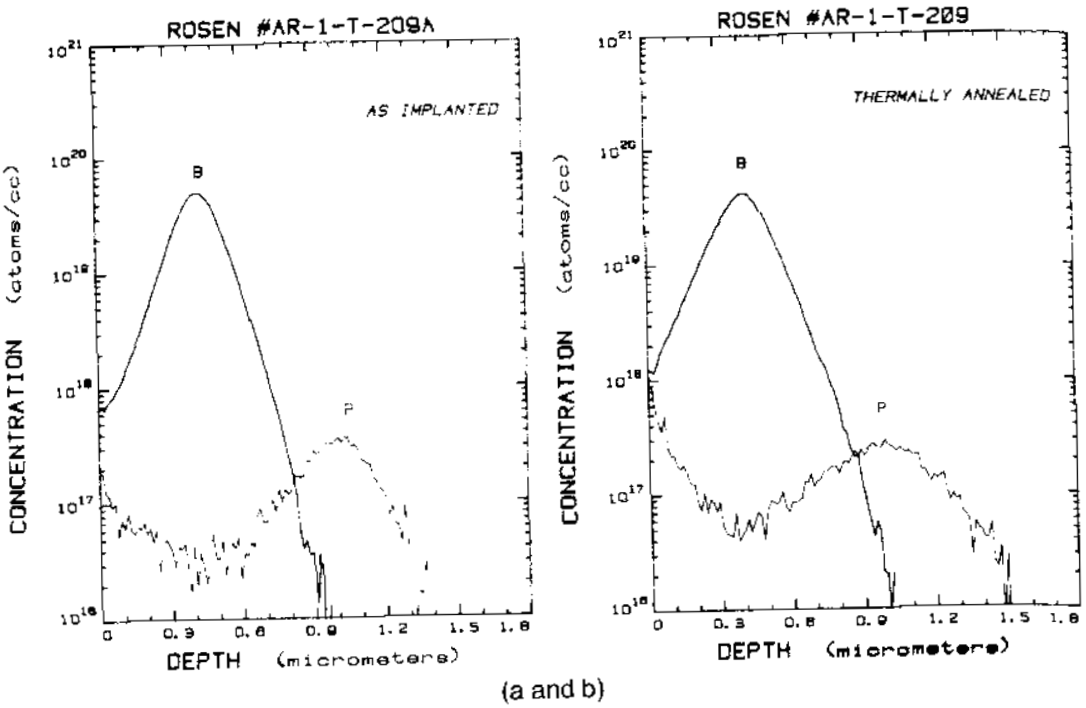
Fig. 15—I-V characteristics of a millimeter-wave IMPATT diode.

of the n-epi should be carefully measured and controlled. The processing is essentially similar to that described in the previous section, except for the insertion of the 0.25 μm n-layer by a $^{31}P^{++}$ ion implantation at 280 keV after the implant for the n^+ contact. The $^{31}P^{++}$ ion implant at 280 keV has the same penetration as a $^{31}P^{+}$ ion implant at 560 keV, which is needed for the deep penetration. Both the n^+ and the n region are laser annealed (simultaneously) as described in the next section.

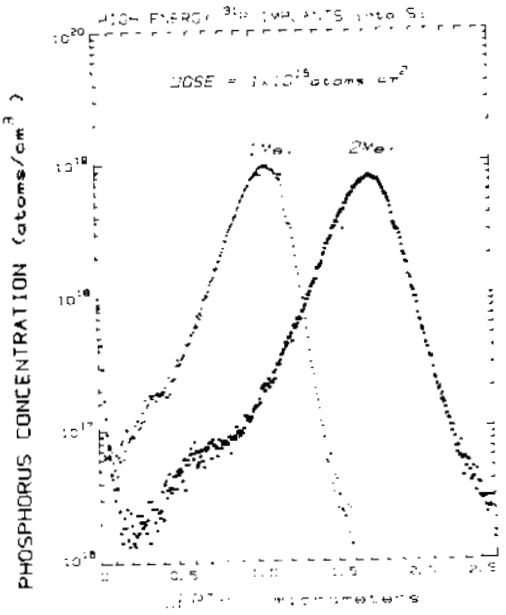
7. Technology Specifics

7.1 Laser Annealing

Laser annealing was performed with a pulsed Nd:YAG laser.[23,40] The laser beam has a pulse width of 15 nanoseconds and contains both the 1.06 μm and the 0.53 μm components. This is achieved by passing the fundamental output of the two-stage pulsed Nd:YAG laser through a Type II KD*P crystal frequency doubler, which has a conversion efficiency of 30%. The dual output pulses are collinear and are optically scanned over the target wafer. The 0.53-μm component has a higher absorption coefficient in silicon. Therefore, electrons and holes generated



(a and b)



(c)

Fig. 16—Results (measured by SIMS) obtained (a and b) on high energy implanting ^{31}P and ^{11}B in silicon before and after annealing and (c) results obtained on ^{31}P implanted into silicon at 1 and 2 MeV.

by the 0.53 μm component enhance the absorption of energy from the 1.06 μm component, which penetrates deeper in silicon and is more suitable for annealing deep implants. The laser beam spot has a diameter of 6 mm, with ~50% overlap between adjacent spots. The pulsed laser is operated at a repetition rate of 10 pulses per second.

Fig. 17 shows the profile distribution determined by SIMS[24-26] of the ion implantation of 50-keV boron into a 10^{16} atoms/cm^3, As-doped,

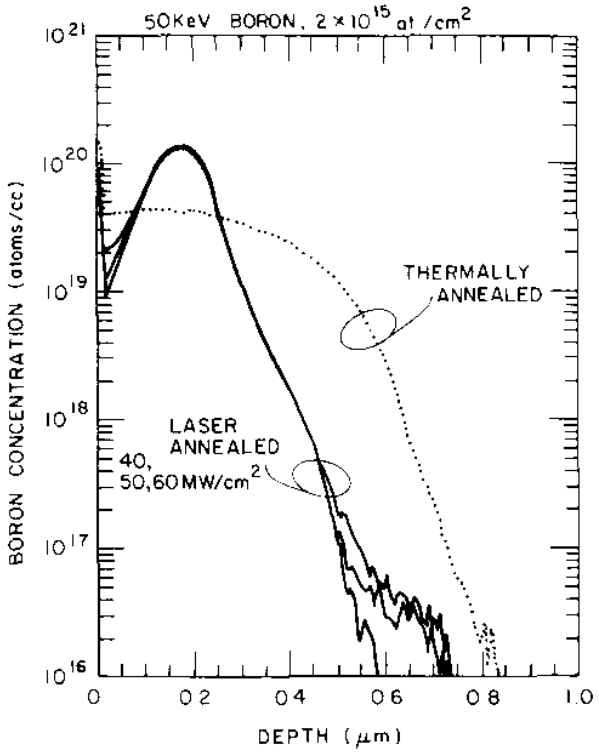


Fig. 17—Profile distribution determined by SIMS comparing effect of laser as opposed to thermal annealing.

epi-grown substrate. The ion-implantation fluence level determines the concentration profiles. The improvement accomplished by the use of laser annealing as opposed to thermal annealing is evident as the sharpness in the profile distribution increases with increasing pulse densities. The ability to obtain the concentration profile by SIMS diagnostics has enabled us to accurately determine the carrier profile resulting from the ion implantation and annealing processes.

7.2 Secondary-Ion Mass Spectrometry

We have built our own instrument[24] for performing secondary-ion mass spectrometry (SIMS). This instrument is particularly well suited for silicon device research because of its Cs^+ primary ion source and its ultra-high vacuum capabilities. We have shown[25] how these attributes have enabled us to profile n-type dopants (P and As) in Si down to concentrations of less than one part per million atomic (ppma). This level of accuracy is normally impossible using a more traditional SIMS instrumentation. Furthermore, we have shown[26] how to depth-profile p- and n-type dopants simultaneously and thus determine electrical junction depths *directly* from the SIMS data. It is this capability that has been of most benefit to millimeter-wave device research. When

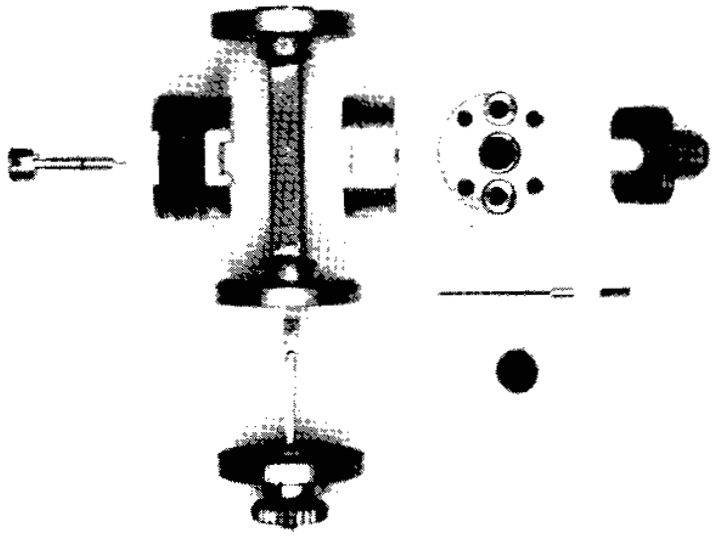


Fig. 18—Disassembled oscillator circuit.

fabricating double-drift diodes by ion implantation, the as-implanted dopant distribution can only be predicted. SIMS is used to measure accurately the p and n dopant distribution after thermal annealing, which is important because diffusion can often alter the profiles in an unpredictable manner, smearing together the very thin layers needed for high GHz operation. We have been successful in determining whether or not the implantation and diffusion steps have produced the desired doping profiles prior to the difficult and tedious steps needed to process the wafers into diodes. SIMS will be of even greater benefit with high-energy (exceeding 1 MeV) ion implantation coupled with laser annealing, because ion ranges at these energy levels are less precisely known and diffusion behavior with laser annealing is, as yet, relatively unpredictable.

7.3 Wafer Thinning

The conventional technique for wafer thinning begins with Cr-Au metallization on the p^+ side to serve as the handle. A hole is opened in the center of the metallization to allow for light transmission measurement to evaluate wafer thickness. The center of the wafer is chemically thinned to as low as 2 μm. The wafer is then supported by the remaining outside ring and the top metallization (with the hole). The thickness of the n-epi

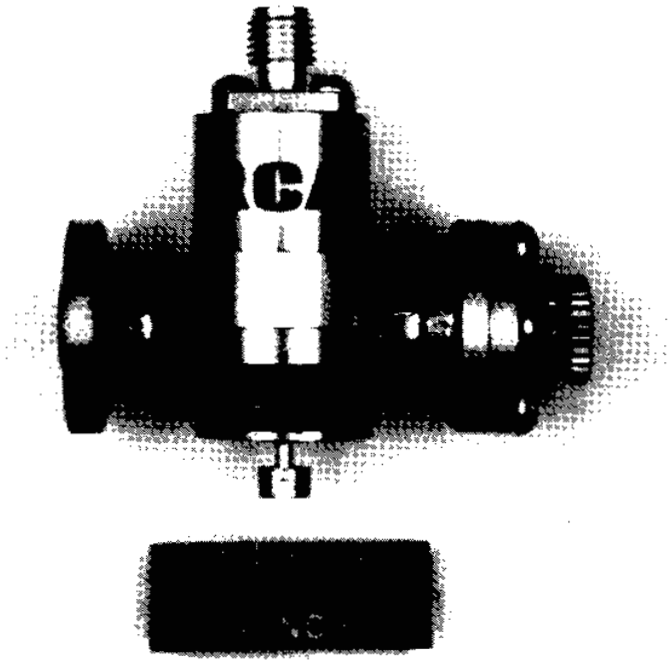


Fig. 19—Reduced-height waveguide circuit.

is then amenable to precision control and measurement.

An extensive investigation of a preferential silicon etch has been launched to enhance our capability to thin substrates uniformly and to selectively remove n^+ material from n.[27]

We have tested an $8CH_3COOH{:}3HNO_3{:}1HF$ solution on ⟨111⟩ orientation, n-type wafers. Wafers with impurity concentrations of 10^{13}, 10^{17}, and 10^{19} atoms/cm^3 were used. Several major factors influence the n etch rate: (1) etching two wafers of different impurity levels simultaneously, (2) the presence of gold metallization, and (3) uniformity of the crystal structure. The 10^{19} atoms/cm^3 (n^+) wafers were the least influenced by these factors, since these wafers etched relatively fast (between 2.7 to 3.5 μm per minute). The etch rates of samples with impurity concentration of less than 10^{18} atoms/cm^3 (n) are significantly lower than 3 μm/min. Several examples of these effects are seen in Table 2. An epi

Table 2—Etch Rates

Impurity Concentration (atoms/cm^3)	Etched Alone (μm/min)	With 10^{19} Sample (μm/min)	With Au Metallization (μm/min)	With Au Metallization and 10^{19} Sample (μm/min)
10^{13}	0.0005–0.0007	0.02	0.04	0.1–0.5
10^{17}	0.003–0.008	0.01	—	0.04
10^{19}	2.7–3.5	2.7–3.5		2.7–3.5

layer of 1.5×10^{15} atoms/cm^3 (on a 10^{19} atom/cm^3, Au-backed substrate) yielded an etch rate of 0.89 μm per minute.

We have achieved repeatability by the careful control of various physical conditions such as total solution volume, temperature, and mix action. Muraoka et al[27] were able to improve results substantially by introducing hydrogen peroxide. We expect this preferential etch to yield suitable etch-rate ratios of at least 10:1 under the worst conditions.

8. Reduced-Height Circuits

Reduced height waveguide circuits[28-30] (Figs. 18 and 19) were used in evaluating the IMPATT diodes. The integrated heat-sink IMPATT was mounted on top of a 16-mil diameter post[31] and connected to a dc bias through a pressure-loaded pin, as shown in Fig. 18. A band-stop filter in the bias line was used to prevent rf leakage at the output frequency. At the end of the dc bias-line, an rf termination constructed of an insulating material providing high rf loss was used. Typical diode-operating conditions at above 100 GHz are V_0 = 14.2 V and I_0 = 111 mA. Device-circuit tuning capabilities are given in Fig. 20.

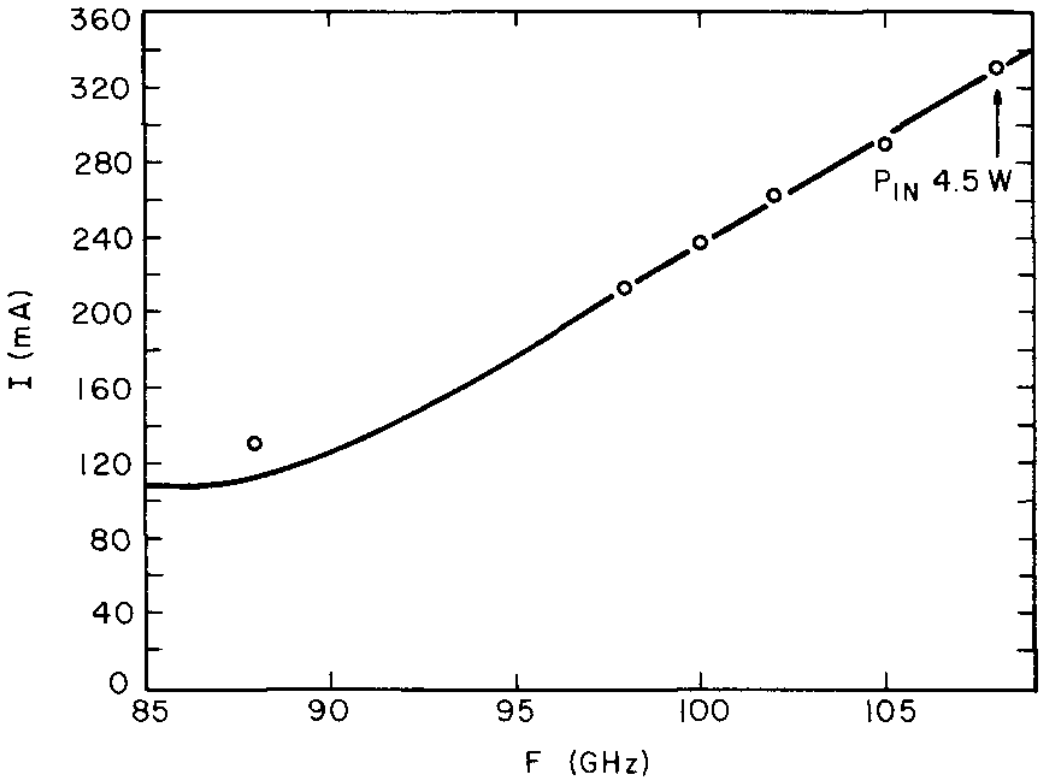


Fig. 20—DC supply current versus IMPATT frequency.

9. Hybrid-Monolithic Circuit Chip

To demonstrate the monolithic-in-silicon concept, we built a 60-GHz oscillator utilizing 5000 ohm-cm silicon wafers as our substrate. This circuit, in addition to a discrete silicon IMPATT device in chip form (Figs. 21 and 22), constitutes what we call the hybrid-monolithic source. To measure the output power of the oscillator, an E-probe microstrip-to-waveguide transition circuit was designed. Preliminary output power obtained is 6.3 mW cw at 56 GHz.

10. Conclusions

On the basis of both theoretical analyses and empirical evidence, silicon appears to be a viable material for millimeter-wave monolithic circuits when advanced device and circuit fabrication techniques are used.

The new technology which we have examined enables us to fabricate ultra thin IMPATT devices without using high-temperature epitaxy and with results that approximate those of the state-of-the-art. The basic techniques involved are (1) all ion-implantation, (2) laser annealing, (3) highly-refined SIMS profile diagnostics, and (4) novel wafer-thinning techniques. Proper application of these techniques, in addition to the propagation properties as measured on microstrip lines using high-resistivity silicon, paves the way for the development of silicon monolithic integrated mm-wave circuits.

Fig. 21—IMPATT diode.

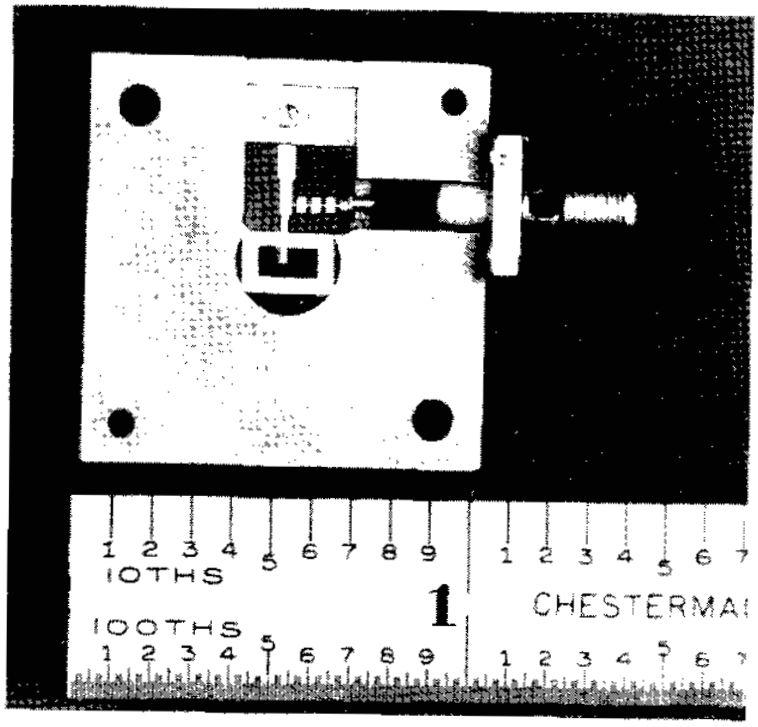


Fig. 22—Millimeter wave hybrid-monolithic circuit on silicon.

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